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EXAMINER	
NATALINI, JEFF WILLIAM	
ART UNIT	**PAPER NUMBER**
2858	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/659,216	CHRISTENSEN, STEEN BAK	
	Examiner	Art Unit	
	Jeff Natalini	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6-16,20,21 and 26-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6-16,20,21,28 and 31-35* is/are rejected.

7)☒ Claim(s) *26,27,29 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/14/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

1. Claims 27, 29, and 30 are objected to because of the following informalities:

- In regard to Claim 27, there seems to be a typo as to which claim it depends from. It states dependency from claim 1, but seems it should be 26 as many dependencies (such as "the parallel format samples" and "the divided down version") all appear in claim 26 and none appear in claim 1.
- In regard to claim 29, it states "wherein the plurality of clock sources comprise", but it has reference to multiple clock signals as well as a second clock source, so this states each of a plurality of clock sources would contain all of the matter claimed in this claim, therefore the system would have at least six clock signals (plurality is at least two, and there are three clock signals defined in the claim- and none of the figures show at least six clock signals). It seems as though this claim should state "The system of claim 1, wherein the second transmitter comprises:" as was the case in previously submitted claim 17.
- Claim 30 is objected to as it depends from claim 29.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 6, 16, 28, and 31-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Searles et al. (2004/01120406) in view of Afshin (EP 1283615).

In regard to claim 1, Searles et al. discloses a first transmitter (fig 3b- 100a) to receive an input signal and to transmit a test signal based on the input signal to a network; a first receiver (200a) to receive a return signal from the network; a second receiver to receive the test signal from the network (200b); and a second transmitter (100b) to receive the test signal from the second receiver using a serial communications line (communication line between 200b and 100b), and where the second transmitter can transfer the test signal as a return signal to the first receiver (communication between the transmitter/receiver combos; abstract and paragraphs 166-117 talk about testing).

Searles et al. lacks wherein the second transmitter reduces jitter in the test signal so it can provide it as the return signal, wherein the second transmitter reduces jitter in the test signal based on clock signals provided by a plurality of clock sources.

Afshin discloses wherein a transmitter that contains a plurality of clock sources (fig 3 (319, 315, 304)) that reduces the jitter compared to the conventional method so that less jitter will be generated in the signal by using these clock sources and associated circuitry (col 9 line 5-15; circuitry is described col 2 line 53 – col 3 line 41).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Searles et al. to incorporate means so as to reduce jitter in

performing tests by using a plurality of clock sources as taught by Afshin in order to increase performance and decrease the needed high speed circuitry (col 9 line 10-17).

In regard to claims 2 and 16, Searles et al. comprises a data processor that provides input signals to the first transmitter (Fig 3a or 3b, 500; paragraph 89), wherein the first receiver is to receive the test/input (these signals are based on each other) signal from the first transmitter using serial communications (communication between 100a and 200a in fig 3b) and wherein the first receiver is to transfer the test/input signal with no additional jitter correction to the data processor (fig 3b transfer to processor 500a) and wherein the data processor is to determine path integrity characteristics based on the input, return, and/or test signal (processor determines relationship between all test data; paragraph 116).

In regard to claim 6, Searles et al. discloses an interface to exchange signals with the data processor (fig 3b (600a or 600b)).

In regard to claim 28, Searles et al. discloses wherein the first receiver (figure 3a (200a)) contains logic to transfer the signal with no additional jitter correction (600a).

In regard to claim 31, Searles et al. discloses wherein the second receiver (figure 3a (200b)) contains logic to transfer the signal with no additional jitter correction (600b).

In regard to claim 32, Searles et al. discloses a first transmitter (fig 3b- 100a) to receive an input signal and to transmit a test signal based on the input signal to a network; a first receiver (200a) to receive a return signal from the network, the first and second receivers make up the first transceiver;

a second receiver (of the second transceiver) to receive the test signal from the network (200b), serially transferring the test signal with no jitter correction as a first signal (600b); and a second transmitter (100b) to receive the test signal from the second receiver, and where the second transmitter can transfer the test signal as a return signal to the first receiver (communication between the transmitter/receiver combos; abstract and paragraphs 166-117 talk about testing).

Searles et al. lacks wherein the second transceiver reduces jitter in the test signal so it can provide it as the return signal, wherein the second transceiver reduces jitter in the test signal based on clock signals provided by a plurality of clock sources.

Afshin discloses wherein a transmitter that contains a plurality of clock sources (fig 3 (319, 315, 304)) that reduces the jitter compared to the conventional method so that less jitter will be generated in the signal by using these clock sources and associated circuitry (col 9 line 5-15; circuitry is described col 2 line 53 – col 3 line 41).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Searles et al. to incorporate means so as to reduce jitter in performing tests by using a plurality of clock sources as taught by Afshin in order to increase performance and decrease the needed high speed circuitry (col 9 line 10-17).

In regard to claim 33 or 35, Searles et al. discloses determining path integrity characteristics based on the input and second or test signals (paragraph 116 determines integrity based on processed signals).

In regard to claim 34, Searles et al. lacks wherein jitter is reduced in the input signal and providing the jitter reduced input signal as the test signal.

Afshin teaches that jitter in any part of the system provides adverse effects, and improving the jitter performance (reducing jitter) increases performance (col 1 line 50-56 and col 9 line 5-17).

It would have been obvious to one with ordinary skill in the art at the time the invention was made to decease jitter in the input signal as taught by Afshin in order to increase performance of the system (col 9 line 5-17).

4. Claims 7-9 and 13-15 rejected under 35 U.S.C. 103(a) as being unpatentable over Searles et al. (2004/01120406) in view of Afshin (EP 1283615), as applied to claims 2 and 6 above, and further in view of Abidin et al. (2004/0100335).

Searles et al. as modified by Afshin lacks specifically stating the interface is compatible with XAUI, IEEE 1394, or PCI and the data processor is in compliance with IEEE 802.3, ITU-T G.709, or ITU-T G.975.

Abidin et al. teaches an interface compatible with XAUI (para 10), IEEE 1394 (para 11), and PCI (para 11) and a processor in compliance with IEEE 802.3 (para 10), ITU-T G.709 (para 10), and ITU-T G.975 (para 10).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Searles et al. as modified to have an interface compatible with XAUI, IEEE 1394, and PCI and the data processor in compliance with IEEE 802.3, ITU-T G.709, and ITU-T G.975, as taught by Abidin et al. in order to be compatible with standards set forth by the industry.

5. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Searles et al. (2004/01120406) in view of Afshin (EP 1283615) as applied to claim 6 above, and further in view of Bass et al. (6449576).

Searles et al. as modified by Afshin lacks, whererin the interface is coupled to a switch fabric (claim 10), packet processor (claim 11), or memory device (claim 12).

Bass et al. teaches wherein the interface (fig 3 (305)) is coupled to a switch fabric (313), packet processor (316), and memory device (308).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Searles et al. as modified to couple a switch fabric to the interface as taught by Bass et al. so that a port mirror of a structure can be utilized to monitor data traffic into and out of network interface (col 6 line 54-62); couple a packet processor to the interface in order to determine the destination of the packet (col 6 line 25-31); couple a memory device to the interface to allow several media ports to receive frames or cells simultaneously where the data is stored temporarily (col 6 line 22-28).

6. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Searles et al. (2004/01120406) in view of Afshin (EP 1283615) as applied to claim 1 above, and further in view of Creigh (6823483).

Searles et al. as modified by Afshin lacks wherein the network includes copper network with the capability to transmit at least at a gigabit per second in accordance with Ethernet.

Creigh teaches a network network includes copper network (col 1 line 60-64) with the capability to transmit at least at a gigabit per second in accordance with Ethernet (col 1 line 24-27).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Searles et al. as modified to have a network comprising gigabit Ethernet over copper as taught by Creigh in order to provide the most dominant technology for LANs (col 1 line 34-35).

Allowable Subject Matter

7. Claim 26 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art does not teach or render obvious where the transmitter comprises a clock and multiplication unit to provide a first clock signal, where the first clock signal is based on a phase comparison between a second clock signal and divided down version of the first clock signal, a phase detector to selectively provided samples of the input signal based on a third clock signal, where the third clock signal is based on the first clock signal, and a second clock source where the second clock signal is based on a phase comparison between the divided down version of the first clock signal and the divided down version of the third clock signal in the combination as claimed.

Response to Arguments

8. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hayssen, III et al. (5630113) discloses using a clock signal in reducing jitter in the system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Natalini whose telephone number is 571-272-2266. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lefkowitz can be reached on 571-272-2180. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeff Natalini

ANJAN DEB
PRIMARY EXAMINER